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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,567	09/12/2003	Kouji Saitou	12480-000021/US	5299
30593	7590	11/15/2006		EXAMINER
				HOLTON, STEVEN E
			ART UNIT	PAPER NUMBER
				2629

DATE MAILED: 11/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)
	10/660,567	SAITOU ET AL.
	Examiner Steven E. Holton	Art Unit 2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

1) Responsive to communication(s) filed on 03 August 2006.  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

4) Claim(s) 1-3 and 6-11 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-3 and 6-11 is/are rejected.  
 7) Claim(s) \_\_\_\_\_ is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____	6) <input type="checkbox"/> Other: _____

## DETAILED ACTION

1. This Office Action is made in response to applicant's amendment filed on 8/3/2006. Claims 1-3 and 6-11 are currently pending in the application. An action follows below:

### *Claim Objections*

2. Claims 1-3 and 6-10 are objected to because of the following informalities: Claims 1-3 and 6-9 use either terms of "optimum voltage", "optimum voltage values", and "voltage values". In light of the previous amendments to claim 1, the Examiner feels that deciding on a uniform term for all of these claims would be helpful for readability of the claims.

Claim 1, uses the phrase "each of which optimum voltage is applied to an electrode having...". The Examiner feels a better phrasing would be "each of the optimum voltages is/may be applied to an..."

Claim 10 uses the term 'a parasite capacitance' in lines 6-7. The Examiner feels a better term would be 'parasitic capacitance' to agree with the common term in the art.

Appropriate correction is required.

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6-8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 6-8, each claim uses similar indefinite language. Claim 6 uses the phrasing "the optimum applied voltage is determined in accordance with a lowest value and a voltage width of the optimum applied voltage". It is unclear what is being measured or considered to generate a lowest value. Is this a lowest value of a measured quantity? The lowest value of a different waveform? The lowest value of a previously applied waveform? Similarly claims 7 and 8 recite 'a highest value' and 'a center value' but it is unclear what is being measured or considered to generate the highest or center values. Further it is unclear in light of the specification exactly how an optimum voltage value could be calculated using it's own width. If the lowest value and the voltage width of a voltage are known, this suggests that the voltage is already known. What computations are done to using the lowest/highest/center value and the voltage width to determine an optimum applied voltage?

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-3 and 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi et al. (USPN: 7084849), hereinafter Noguchi, in view of Koyama (USPN: 6600465).

Regarding claim 1, Noguchi discloses a liquid crystal display device where an offset voltage is applied for matching the center level of the signal electrode to the center level of the common electrode waveform (Fig. 23; col. 38, lines 18-39). However, Noguchi does not expressly disclose if the offset voltage is generated or stored by the display before being applied to the signals applied to the electrodes.

Koyama discloses a liquid crystal display device that measures a offset value to be applied to display electrodes of the device. The offset voltages are stored in a memory device (Fig. 1, element 103) and then read from the memory to be applied to the correct electrodes (col. 3, lines 50). Koyama also discusses that the storage device could be either a digital memory or an analog circuit to generate the offset voltage (col. 3, lines 19-28).

At the time of invention it would have been obvious to one skilled in the art to modify the teachings of Noguchi with the teachings of Koyama to produce a device as

described in claim 1. A digital memory device as described by Koyama could be used to store offset voltages that would be read out for the purpose of matching the center voltages of the common and source electrodes as used by Noguchi. Noguchi does not describe how the offset voltages are generated or stored and thus, any reasonable method of providing offset voltages to electrodes could be used by one skilled in the art. One such known and reasonable method of providing offset voltages to electrode waveforms for display devices is a digital memory as shown by Koyama. Thus, it would have been obvious to one skilled in the art to modify the teachings of Noguchi with the teachings of Koyama to produce a device as described in claim 1.

Regarding claim 2, Noguchi discloses changing the signal electrode waveform to match the center of the common electrode. Noguchi also discloses a similar method of applying an offset voltage to the common electrode to alter the waveform of the common electrode (col. 35, lines 33-40). Using the teachings of Noguchi it would have been obvious to one skilled in the art that either the common electrode waveform or the signal electrode waveform could be shifted using an offset voltage. The result of the offset, to either match or unmatch the center of voltage waveforms, would be a matter of design choice and it would have been obvious that instead of providing the offset voltage to the signal electrode to match center voltages, the offset could be applied to the common electrode as described in claim 2.

Regarding claims 3 and 9, Noguchi discloses using an offset voltage to match the center of voltage waveforms applied to the signal and common electrodes and the

shift does not include a change of the amplitude of the voltage waveform being shifted (col. 38, lines 18-39).

Regarding claim 10, the display device of Noguchi includes thin film transistors (Fig. 1, element 20; col. 11, line 55) the transistors are connected to signal lines, gate signal lines and connected to the pixel as is common in active matrix display devices. The matching of the centers of the signal and common electrode waveforms is used to overcome a voltage that is stored in the pixel because of parasitic capacitance between components of the pixel (col. 35, lines 22-40).

Regarding claim 11, the display of Noguchi is a dual-mode display that operates with a reflective and transmissive mode of operation (col. 2, lines 32-46).

#### ***Response to Arguments***

5. Applicant's arguments with respect to claims 1-3, and 6-11 have been considered but are moot in view of the new ground(s) of rejection based on the amendments and newly found prior art.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven E. Holton whose telephone number is (571) 272-7903. The examiner can normally be reached on M-F 8:30-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven E. Holton  
Division 2629  
November 9, 2006

AMR A. AWAD  
SUPERVISORY PATENT EXAMINER  
